REMARKS

Favorable reconsideration of this application in view of the remarks to follow and allowance of the claims of the present application are respectfully requested.

In the Advisory Action dated July 18, 2005, Claims 1-4, 8-9, 11-12 and 14-15 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent Application Publication No. 2002/0125575 to Chaen (hereinafter "Chaen"). Specifically, the Examiner alleges that although the lower metal layer is not mentioned in Chaen, it does not mean the disclosed metal layer 6 is not an upper metal layer since the metal layer 6 is connected with the upper part of the device.

Applicants respectfully submit that Chaen does not teach the claimed semiconductor structure recited in Claim 1. Specifically, Chaen does not disclose a metal stacked inductor comprising at least one first layer of metal which serves as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal, wherein said first layer of metal and said second layer of metal are not interconnected by a via.

First, applicants believe it is important to note the differences between a metal wire and a metal layer in a semiconductor structure. A metal wire denotes a metal conductor that carries electricity over a distance, while a metal layer refers to a relatively thin sheet-like metal expanse or region lying over or under another layer. A metal layer in a semiconductor device may or may not be a metal wire. Specifically, a metal layer can be a metal wire only when said metal layer serves the function of conducting electricity.

Turing to the present invention, as shown in FIG. 2, the first metal layer 52 of the metal stacked inductor is formed within a first dielectric material 58 that is formed on top of a

lower metal wiring level 64 (see also paragraph [0034]). The lower metal wiring level 64 is formed on top of the substrate 62 and comprises a dielectric 66 that includes a lower metal wire 68 embedded therein. Notably, the lower metal wiring level 64 is in electrical contact with the first metal layer 52 by via 69. That is, the first metal layer 52 not only serves as the bottom metal layer of the metal stacked inductor, but it also serves as the upper metal wire of the interconnect structure.

In Chaen, the lower metal layer 6 is formed on top of an insulating film 4, which is formed on top of the substrate 2 (FIG. 2). Inasmuch as an insulating material has negligible electrical conductivity, the insulating film 4 cannot serve as a lower metal wiring as the layer 64 of the present application does. That is, the insulating film 4 prevents the lower metal layer 6 from electrically contacting any other layers or device beneath the insulating film 4. Since the lower metal layer 6 is the bottom metal layer of the stacked metal structure disclosed in Chaen and does not have electrical contact with any other layers underneath, the lower metal layer 6 in Chaen does not serve as an upper metal wire of the interconnect structure as the claimed first metal layer 52 does. Thus, the claimed semiconductor structure is distinct from that of Chaen.

It is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. *In re King*, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Since the Chaen device is structurally and functionally different from the claimed semiconductor structure, Chaen does not anticipate the present invention.

The rejection under 35 U.S.C. §102(b) has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Claims 5-7 and 19-20 stand rejected under 35 U.S.C. §103(a), as allegedly unpatentable over Chaen in view of U.S. Patent No. 6,395,637 to Park et al. (hereinafter "Park"). More specifically, the Examiner alleges that Chaen teaches substantially the entire structure of Claim 1, and Park teaches the first layer metal in connected to a lower metal wiring level. The Examiner therefore concludes that it would have been obvious to one skilled in the art at the time the invention was made to incorporate the lower level of wiring taught by Park in the structure of Chaen to integrate the inductor structure with other regions of the device.

Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness as discussed below.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the cited reference must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the reference, not based on applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

First, applicants believe that the cited references, solely or in combination, do not teach or remotely suggest the claimed structure. Chaen discloses an inductor comprising a plurality of metal layers stacked on a first insulating layer, but the lower-most metal layer 6 does not serve as a wiring level as in the claimed structure. Park discloses a metal stacked inductor comprising three layers of metal. However, there is a dielectric layer and a via hole between the metal layers. In other words, the second layer of metal connects to the first layer of metal by a via, and the third layer of metal connects to the second layer of metal by a via. In contrast,

Claim 1 of the present invention specifies that the second layer of metal and the first layer of the metal are not interconnected by a via, and the first layer of metal, i.e., the bottom metal layer, serves as the upper metal wire of the interconnect structure. Thus, Chaen and Park, solely or in combination, do not teach or remotely suggest the present invention.

Second, applicants submit that the cited references do not teach, suggest or motivate one skilled in the art to modify the disclosed devices to arrive at the present inventive semiconductor structure. Chaen states that the inductor disclosed therein is structured to prevent collapse and delamination of an inductor without increasing an occupied area or to further reduce the area of the inductor while preventing the collapse and delamination (paragraph [0011] of Chaen). However, there is no suggestion in Chaen which motivates one skilled in the art to modify the disclosed device so that the bottom metal layer serves as the upper metal wire of a interconnect structure. Park emphasizes that the high performance of the inductor is achieved by fully filling the via hole and the via recesses with the Al layer to increase the actual thickness of the inductor coil (lines 9-21, column 6), while the claimed structure recites that the second layer of metal and the first layer of the metal are not interconnected by a via. Thus, Park teaches away from the present claimed structure.

Further, applicants believe that in view of the cited references, one skilled in the art would not have any reasonable expectation of success to incorporate the lower level of wiring taught by Park in the structure of Chaen. As discussed previously, Chaen disclose a semiconductor structure to prevent collapse and delamination of an inductor without increasing an occupied area or to further reduce the area of the inductor (paragraph [0011] of Chaen), while the present invention provides an integrated metal stacked inductor that has a high quality factor Q, yet has a substantially low sheet resistance (paragraph [0015] of the specification). Further,

the thickness of metal layers of the present invention is preferred to be similar (paragraphs [0053], [0057], and [0062] of the specification), while the thickness of metal layers **12, 10** and **6** is 4.5 uM, 250 nm, and 200 nm, respectively (paragraphs [0044], [0033], and [0031] of Chaen). Moreover, the second metal layer in Chaen, i.e., metal layer **10**, is not planar (FIG. 2 of Chaen), while the second metal layer of the present invention does not have any required topography. Park discloses a metal stacked inductor comprising three layers of metal and emphasizes that the high performance of the inductor is achieved by fully filling the via hole and the via recesses with the Al layer to increase the actual thickness of the inductor coil (lines 9-21, column 6). Thus, in view of Chaen, which discloses a structure to improve the structural strength of an inductor, and Park, which discloses a structure using via holes and via recesses to achieve high performance, one skilled in the art would not reasonably expect a structure incorporating the lower level of wiring taught by Park in the structure of Chaen, which does not have via holes or via recesses, can achieve high performance.

Accordingly, applicants submit that in view of the cited references at the time the invention was made, one skilled in the art would not obviously envision metal stacked inductor comprising at least one first layer of metal which serves as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal, wherein said first layer of metal and said second layer of metal are not interconnected by a via. Thus, Claims 5-7 and 19-20 are not rendered obvious by Chaen in view of Park.

Claims 10 and 13 stand rejected under 35 U.S.C. §103(a), as allegedly unpatentable over Chaen in view of U.S. Patent No. 6,639,298 to Chaudhry, et al. (hereinafter "Chaudhry"). Particularly, the Examiner alleges that Chaen teaches substantially the entire structure of Claim 1, and Chaudhry teaches the use of Cu in the process of forming a multi-layer

inductor structure. The Examiner therefore concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use copper in the structure of Chaen as taught by Chaudhry in order to form a high Q inductor.

Claims 16-17 stand rejected under 35 U.S.C. §103(a), as allegedly unpatentable over Chaen in view of Park. Claim 18 stands rejected under 35 U.S.C. §103(a), as allegedly unpatentable over Chaen, Chaudhry in view of Park. More specifically, the Examiner alleges that Chaen teaches substantially the entire structure of Claim 1, Park teaches a third metal layer that is made of aluminum, and Chaudhry teaches using Cu in the process of forming a multi-layer inductor structure. The Examiner therefore concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine both Cu and Al as taught by both Park and Chaudhry in the structure of Chaen in order to form a high Q inductor.

Applicants respectfully submit that Claims 10, 13, and 16-18 of the present application are not rendered obvious by Chaen in view of Park and Chaudhry because the applied references do not teach or remotely suggest applicants' claimed semiconductor structure. Specifically, the applied references, solely or in combination, do teach or suggest the claimed metal stacked inductor comprising at least one first layer of metal which serves as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal, wherein said first layer of metal and said second layer of metal are not interconnected by a via. Chaudhry, discloses an integrated circuit inductor having a plurality of insulating layers and a plurality of metallization layers, which differs considerably from the claimed metal stacked inductor. As discussed previously, Chaen discloses an inductor comprising a plurality of metal layers stacked on a first insulating layer, but the lower-most metal layer 6 does not serve as wiring levels as in the claimed structure. Park emphasizes that

the high performance of the inductor is achieved by fully filling the via hole and the via recesses with the Al layer to increase the actual thickness of the inductor coil (lines 9-21, column 6), while the claims specify that the second layer of metal and the first layer of the metal are not interconnected by a via.

Furthermore, the cited references fail to suggest the present semiconductor structure. While Chaen states that the semiconductor structure disclosed therein is intended to prevent collapse and delamination of an inductor without increasing an occupied area or to further reduce the area of the inductor while (paragraph [0011] of Chaen), Chaudhry specifically teaches that the desirable low-resistance (and thus high Q) of the inductors is achieved by using a dual damascene process to form such an inductor (lines 56-67, Column 2 of Chaudhry). Notably, the present specification states that the high performance of the claimed inventive inductor having substantially low sheet resistance is achieved because no via is used interconnecting the multiple layers of metal (paragraphs [0018] and [0019] of the specification). As discussed previously, Park teaches away from the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification suggested by the Examiner. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested. Thus, in view of the foregoing remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

Leslie S. Szivos, Ph.D.
Registration No. 39,394

Scully, Scott, Murphy & Presser
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343

LSS/YL:dg